

Atty. Dkt. No. 039153-0460 (G1165)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Buynoski et al.

Title: METHOD OF SELF-ANNEALING CONDUCTIVE LINES THAT SEPARATES GRAIN SIZE EFFECTS FROM ALLOY MOBILITY

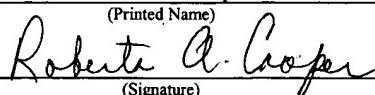
Appl. No.: 10/628,733

Filing Date: 07/28/2003

Examiner: Joannie A. Garcia

Art Unit: 2823

Conf. No.: 4021

<b>CERTIFICATE OF EXPRESS MAILING</b>	
I hereby certify that this correspondence is being deposited with the United States Postal Service's "Express Mail Post Office To Addressee" service under 37 C.F.R. § 1.10 on the date indicated below and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
EV 505573021 US (Express Mail Label Number)	08/25/04 (Date of Deposit)
Roberta A. Cooper (Printed Name)	
 (Signature)	

**DECLARATION UNDER 37 C.F.R. § 1.131**

Commissioner for Patents  
PO Box 1450  
Alexandria, Virginia 22313-1450

Sir:

We, Matthew S. Buynoski, Connie Pin-Chin Wang, Paul R. Besser, and Minh Q. Tran state and declare that:

1. Each of us is an inventor of at least one of Claims 1-20 currently pending in U.S. Patent Application No. 10/628,733 titled "METHOD OF SELF-ANNEALING CONDUCTIVE LINES THAT SEPARATES GRAIN SIZE EFFECTS FROM ALLOY MOBILITY" (hereinafter "the '733 application").

2. We understand that in an Office Action dated July 8, 2004, each of Claims 1-20 were rejected as being unpatentable in view of U.S. Patent No. 6,660,633 to Lopatin et al. titled "METHOD OF REDUCING ELECTROMIGRATION IN A COPPER LINE BY ELECTROPLATING AN INTERIM COPPER-ZINC ALLOY THIN FILM ON A COPPER SURFACE AND A SEMICONDUCTOR DEVICE THEREBY FORMED" (hereinafter "Lopatin et al.").

3. We understand based on the information provided on the front page of Lopatin et al. that Lopatin et al. has a filing date of February 26, 2002.

4. At least by August 21, 2001, we conceived in the United States the ideas set forth in Claims 1-20 of the '733 application. Such conception is evidenced by the attached

Exhibit A, which is an invention disclosure form pertaining to the subject matter of the present application.

5. Based on the conception of the ideas set forth in Claims 1-20 at least by August 21, 2001, the subject matter recited in Claims 1-20 was invented by us prior to the February 26, 2002 filing date of Lopatin et al.

6. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are true, and further that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application or any patent issuing therefrom.

Date: 12 August 2004 By: Matthew S. Buynoski  
Matthew S. Buynoski

Date: 8/23/04 By: Connie Pin-Chin Wang  
Connie Pin-Chin Wang

Date: 8/18/04 By: Paul R. Besser  
Paul R. Besser

Date: 8/23/04 By: Minh Q. Tran  
Minh Q. Tran

TUESDAY, AUGUST 21, 2001  
**COPPER ALLOY PATENT HARVESTING SESSION**  
 GROUP 1: ROOM C-617  
 Technical Leader: Connie Wang  
 TOPIC: PROCESS

#72  
**PRIORITY**  
 A  B   
 C  D

-9

**AMD INVENTION DISCLOSURE**

TLD ID# **G1165** Rec'd date \_\_\_\_\_  
 Sunnyvale x42110, return to MS68, Texas x55964 return to MS62

Project:  Product:  Process:  Technology , to which the invention applies (*identify*):

List 2 to 5 key words useful to search by to find patents or art related to this invention:

Working title of invention: *Separating Cu grain size effects from alloy visibility  
by use of soft annealing*

→INVENTOR/SESSION PARTICIPANT ADDRESS INFORMATION IS ON THE NEXT PAGE (IA)←

Inventor's signature: *Muth Lee Buynosu* date: \_\_\_\_\_

Inventor's printed full name: *Muth Lee Buynosu* Citizenship: \_\_\_\_\_

Employee #: \_\_\_\_\_ Extension: \_\_\_\_\_ Mail stop: \_\_\_\_\_ Home telephone: ( ) \_\_\_\_\_

Division: \_\_\_\_\_ Directorate: \_\_\_\_\_ Dept #: \_\_\_\_\_ Dept : \_\_\_\_\_ Manager: \_\_\_\_\_

Residence address: \_\_\_\_\_

Post Office address: \_\_\_\_\_

Co-Inventor's signature: \_\_\_\_\_ date: \_\_\_\_\_

Co-Inventor's printed full name: \_\_\_\_\_ Citizenship: \_\_\_\_\_

Employee #: \_\_\_\_\_ Extension: \_\_\_\_\_ Mail stop: \_\_\_\_\_ Home telephone: ( ) \_\_\_\_\_

Division: \_\_\_\_\_ Directorate: \_\_\_\_\_ Dept #: \_\_\_\_\_ Dept : \_\_\_\_\_ Manager: \_\_\_\_\_

Residence address: \_\_\_\_\_

Post Office address: \_\_\_\_\_

Co-Inventor's signature: \_\_\_\_\_ date: \_\_\_\_\_

Co-Inventor's printed full name: \_\_\_\_\_ Citizenship: \_\_\_\_\_

Employee #: \_\_\_\_\_ Extension: \_\_\_\_\_ Mail stop: \_\_\_\_\_ Home telephone: ( ) \_\_\_\_\_

Division: \_\_\_\_\_ Directorate: \_\_\_\_\_ Dept #: \_\_\_\_\_ Dept : \_\_\_\_\_ Manager: \_\_\_\_\_

Residence address: \_\_\_\_\_

Post Office address: \_\_\_\_\_

Co-Inventor's signature: \_\_\_\_\_ date: \_\_\_\_\_

Co-Inventor's printed full name: \_\_\_\_\_ Citizenship: \_\_\_\_\_

Employee #: \_\_\_\_\_ Extension: \_\_\_\_\_ Mail stop: \_\_\_\_\_ Home telephone: ( ) \_\_\_\_\_

Division: \_\_\_\_\_ Directorate: \_\_\_\_\_ Dept #: \_\_\_\_\_ Dept : \_\_\_\_\_ Manager: \_\_\_\_\_

Residence address: \_\_\_\_\_

Post Office address: \_\_\_\_\_

List on additional sheet if there are more co-inventors and list total number of inventors here: \_\_\_\_\_

Name(s) of attorney(s) preferred by inventor(s) to prepare patent application, if known:

**LAW FIRM: FOLEY & LARDNER**  
**ATTORNEYS: Paul Hunter and Joe Ziebert**

Witness 1 initial: \_\_\_\_\_ Witness 2 initial: \_\_\_\_\_

TDG-Copper Alloy Patent Harvesting Session  
Group 1 Topic: Process Issues

Technical Leader: Pin-Chin Connie Wang  
Law Firm: Foley & Lardner (Paul Hunter & Joe Ziebert)

**PARTICIPANT ADDRESSES**

Tuesday, August 21, 2001—ROOMS C-6&7

Exhibit A

Name	Citizenship	Employee #	Dept. #	Mail Stop	Work #	Fax #	Address	City	State	Zip Code
Besser, Paul R. Paul.Besser@amd.com	USA	023186	07198	160	408/749-2350	408/749-5144	1087 Yorktown Drive	Sunnyvale	CA	94087
Buynoski, Matthew S. Matthew.Buynoski@amd.com	USA	022264	07016	117	408/749-4077	408/749-2953	2607 Emerson Street	Palo Alto	CA	94306
Lopatin, Sergey D. Sergey.Lopatin@amd.com	BELARUS	024895	07198	160	408/749-5175	408/749-5144	1000 Kiely Blvd #66	Santa Clara	CA	95051
Myers, Alline F. Alline.Myers@amd.com	USA	025301	07370	32	408/749-3928	408/774-8812	121 Saratoga Ave #4206	Santa Clara	CA	95051
Romero, Jeramias D. Jeramias.Romero@amd.com	USA	021249	07370	32	408/749-5889	408/774-8812	30077 Bridgeview Way	Hayward	CA	94544
Tran, Minh Q. Minh.Tran@amd.com	USA	024375	07198	79	408/749-3104	408/749-3851	1722 Mirabella Court	Milpitas	CA	95035
Wang, Pin-Chin Connie Connie.Wang@amd.com	TAIWAN	025191	07198	117	408/749-2687	408/749-5144	461 Burgess Drive #2	Menlo Park	CA	94025
You, Lu Lu.You@amd.com	PEOPLE'S REPUBLIC OF CHINA	023537	07198	160	408/749-6589	408/749-5144	5978 Friar Way	San Jose	CA	95129

**IDF PAGE 1A**

**AMD INVENTION DISCLOSURE**

TLD ID# \_\_\_\_\_

Rec'd date \_\_\_\_\_

California x42110, return to MS68,

Texas x55964 return to MS562,

Dresden x83401 Silke Kretzschmar at MS E21-PP.

Identify known relevant art (patents, publications, products):

Give a well-known, well-known, Sett-anneal at room temp  
Following electroplated depositions

State the problem solved by this invention: Blocking of ~~the~~ electromigration by alloying elements in the crossing grain boundaries ~~is~~ dependent on the Cu grain size + alloying element diffusion kinetics. This separates them.

Brief description and/or sketch of invention (please attach copies of AMD patent notebook pages, reports or drawings):

Instead of using a furnace at temp 250-350°C to anneal the grains, the Cu metal is "sett-annealed" at a higher from ambient temperature for 24-48 hrs to <100°C for 8-24 hrs. There is no appreciable motion of alloying element when the ~~area~~ Cu re-crystallization occurs. Anneal conditions in subsequent furnace anneal can now be tailored exclusively to needs of distributing the alloying element, without ~~the~~ affecting the Cu grain structure. Also, fewer grain boundaries (post sett-anneal) result in a given amount of alloying element being more concentrated in the grain boundaries, requiring use of less alloy element in total to reach an effective level. This leads to lower overall line resistance.

Patent notebook # \_\_\_\_\_ Page numbers \_\_\_\_\_

Number of drawings \_\_\_\_\_

Witness 1 initial: \_\_\_\_\_

Witness 2 initial: \_\_\_\_\_

**AMD INVENTION DISCLOSURE**

TLD ID# \_\_\_\_\_

Rec'd date \_\_\_\_\_

California x42110, return to MS68,

Texas x55964 return to MS562,

Dresden x83401 Silke Kretzschmar at MS E21-PP.

Advantages (check all that apply):

<input type="checkbox"/> avoids existing patent(s)	<input type="checkbox"/> improves precision	<input type="checkbox"/> simplifies manufacturing
<input type="checkbox"/> new function	<input type="checkbox"/> improves accuracy	<input type="checkbox"/> improves wear characteristic
<input type="checkbox"/> improves density	<input type="checkbox"/> improves efficiency	<input type="checkbox"/> improves signal to noise ratio
<input type="checkbox"/> increases operating speed	<input type="checkbox"/> fewer component parts	<input type="checkbox"/>
<input type="checkbox"/> improves reliability	<input type="checkbox"/> reduces cost of manufacturing	<input type="checkbox"/>

Discussion of advantage of the invention over other solutions

(emphasize technical advance in the art as measured against known art):

First written description* of invention, date:	First external disclosure to (name):
Date of first drawing*:	Date of first external disclosure, none <input type="checkbox"/>
Date invention first reduced to practice:	External disclosure under NDA* No <input type="checkbox"/> Yes <input checked="" type="checkbox"/>
Made by (name):	First external disclosure or use by: presentation <input type="checkbox"/>
Tested by (name):	announcement <input type="checkbox"/> , sample <input type="checkbox"/> , sale <input type="checkbox"/> , other <input type="checkbox"/>
Date of first computer simulation:	Date of Non-Disclosure Agreement*, if any:
Date of first successful test:	Date of first publication*:
any of above occurred outside of USA <input type="checkbox"/>	Publication name:
* attach copy if possible	Date of first commercial use:

Does plan exist to publish, disclose or sell? If so, where and when?

Was invention conceived, constructed or tested pursuant to the performance under a development contract with another company: No  Yes  If yes, company name \_\_\_\_\_

If yes, name of AMD business contact and contract no. \_\_\_\_\_

Was invention jointly developed with participation of inventors from outside AMD: No  Yes 

If yes, Company name \_\_\_\_\_

I have read and understood this disclosure and read and signed each page of the attachments:

Witness 1 signature: \_\_\_\_\_ Date: \_\_\_\_\_  
Printed name: \_\_\_\_\_ Employee #: \_\_\_\_\_Witness 2 signature: \_\_\_\_\_ Date: \_\_\_\_\_  
Printed name: \_\_\_\_\_ Employee #: \_\_\_\_\_

After completing to this point, deliver to department reviewer. Date delivered: \_\_\_\_\_

Witness 1 initial: \_\_\_\_\_ Witness 2 initial: \_\_\_\_\_

**AMD INVENTION DISCLOSURE**

TLD ID# \_\_\_\_\_

Rec'd date \_\_\_\_\_

California x42110, return to MS68,

Texas x55964 return to MS562,

Dresden x83401 Silke Kretzschmar at MS E21-PP.

**DISCLOSURE EVALUATION (Entries from this point on are by the Reviewer)**Does this invention add value to the AMD intellectual property portfolio? Yes , No ,

Explain:

Do you know of any relevant art? Yes , No , If yes, attach a copy and explain: \_\_\_\_\_

What application(s) do you foresee for this invention? \_\_\_\_\_

I estimate the Value\* of this invention disclosure is A , B , C , D 

\* use worksheet "Valuing Invention Disclosures and Patents".

it is , is not  recommended to AMD for U.S. patent application filing,it is , is not  recommended to AMD for foreign patent application filing,it is , is not  recommended to be held as an AMD trade secret,Give this high priority , normal , low priority , in patent application writing.**GUIDELINES AND CONSIDERATIONS FOR FOREIGN FILING DECISION**

Filing foreign patent applications is costly. We should choose to do it only when conditions warrant.

**ALL CONDITIONS BELOW MUST APPLY IN ORDER TO INITIATE A FOREIGN FILING:**

- *Invention is High-Valued (A, B)\*, and*
- *Invention is in our technology path (usage), and*
- *Invention usage is detectable by inspection of product, and*
- *Invention is relatively hard to design around, and*
- *Competitor is operating in the country of interest. ( see ca000000.xls tabulation of "Factory Sites outside the USA .)*

I recommend filing patent applications in foreign countries checked below:

Japan <input type="checkbox"/>	S.Korea <input type="checkbox"/>	Taiwan <input type="checkbox"/>	U.K. <input type="checkbox"/>	France <input type="checkbox"/>	Germany <input type="checkbox"/>
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

Reviewer's signature: \_\_\_\_\_ Employee #: \_\_\_\_\_ Date: \_\_\_\_\_

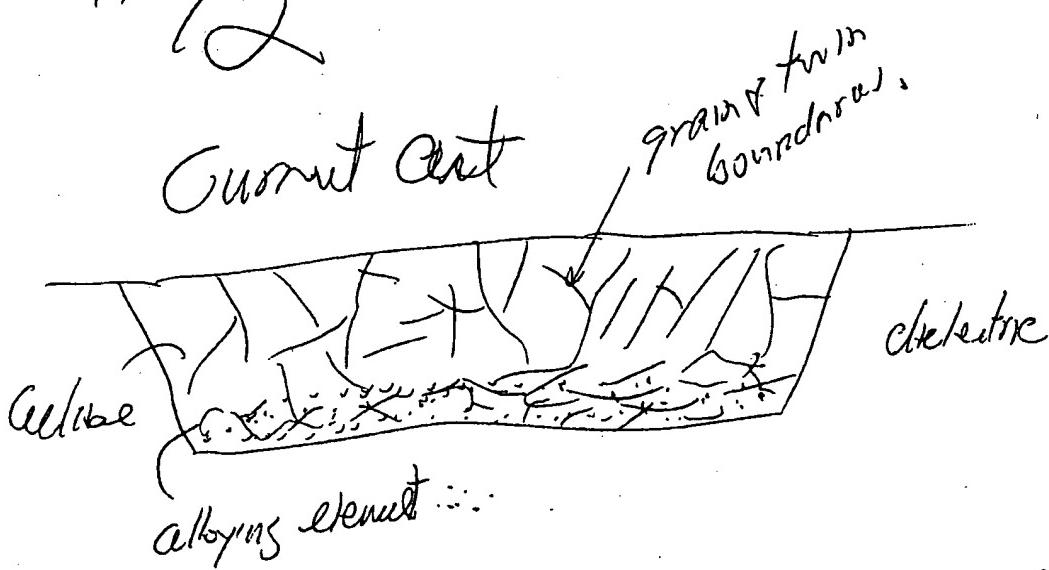
Reviewer's printed name: \_\_\_\_\_

If foreign filing is checked, route to Div. VP for signature.

VP or Designate approves foreign filing (signature) \_\_\_\_\_

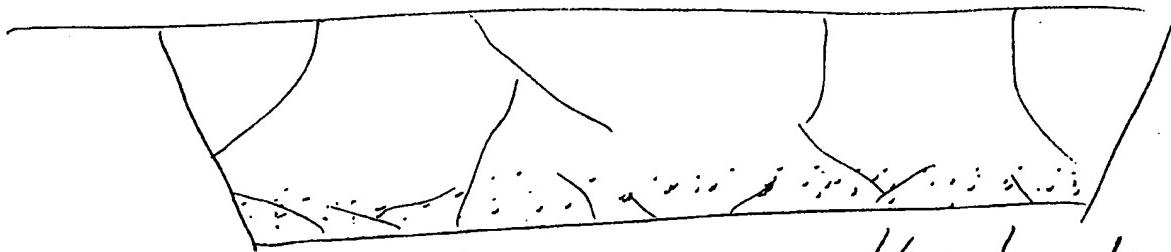
Reviewer: Complete this page and send disclosures to TLD for patent application filing.

#72



Alloying element moves up large # of grain boundaries  
& may prevent some from being destroyed during anneal.

Proposed - as line after soft-anneal



Alloying element has finer grain/twin boundaries to fill up & passivate. Overall, finer boundaries mean less chance for grain/boundary diffusion.